interconnection layer **60** may be formed by means of a thin-film deposition technique such as sputtering using a mask. Referring to FIG. 3D, a nickel plating **62** is made on the aluminum interconnection layer **60**. The nickel plating has a thickness of at least about 5 micrometers in order to absorb any thermal stress generated due to the difference in coefficient of thermal expansion between the final semiconductor device and a circuit board on which the semiconductor device is to be mounted. The thickness of the nickel plating **62** also affects the reliability of the joint between the nickel surface and a bump electrode formed later. In this embodiment, the nickel plating has a thickness of 10 micrometers. The plating on the aluminum interconnection layer **60** is not limited to nickel, and other metals such as copper may be used, provided that they have the desired adhesion and diffusion barrier properties, as a barrier metal, the material of the bump electrodes (solder in this embodiment).

Referring to FIG. 3E, a cover coating film **64** is applied on the nickel plating **62** and the passivating film **12**. The cover coating film **64** may be made of, for example, polyimide applied to have a thickness of 20 micrometers or smaller. This cover coating film **64** is similar in function to the organic insulation film **31** of the carrier film **30** described in conjunction with the conventional process. Next, a number of apertures **66** are formed in the cover coating film **64**. The position of the apertures **66** corresponds to where the bump electrodes described below are formed. Accordingly, the position of the apertures **66** is not limited to a specific embodiment and may be selected depending on applications of the resultant semiconductor device. The aperture **66** is formed by means of, for example, etching (mechanical or laser) to the extent that the surface of the nickel plating **62** is exposed to the atmosphere. Subsequently, a gold plating **68** is made on the exposed surface of the nickel plating **62**. Though not necessarily formed, the gold plating **68** is preferable for a higher reliability of the bump electrodes.

Referring to FIG. 3F, bump electrodes **70** are formed in the aperture **68** and on the surface of the cover coating film **68**. The bump electrode **70** may be generally spherical or hemispherical and about 100 micrometers high, but different shapes may be used. This bump electrode **70** may be made according to the following steps. A solder piece is cut from a solder strip by using a die and a punch. This solder piece is adhered in the aperture **66** using an adhesive material such as rosin (flux). The solder piece is then heated and melted to form the bump electrode. The rosin is washed out after the formation of the bump electrodes **70**.

The wafer at this stage is illustrated in FIGS. 4A through 4C. As apparent from the figures, the bump electrodes **70** are formed on the entire surface of the wafer **10** except for there the scribe lines are defined. In addition, the aluminum interconnection layer **60** is extending at the position of the aperture **66**. Though the bump electrodes **70** in this embodiment are formed on the wafer except for the portions just under which the chip electrodes **11** are formed, the bumps **70** may be formed over the chip electrodes **11**.

Turning to FIG. 3G, the semiconductor chip sections defined on the wafer **10** are separated from each other into individual semiconductor devices **80** by means of dicing.

The conventional wafer **10'** illustrated in FIG. 1A has the chip electrodes **11** away from each other at a pitch of approximately 0.1 mm. The resultant semiconductor device thus has the bump electrodes away from each other at the same pitch of 0.1 mm or smaller. On the contrary, the pitch can be increased up to approximately 0.5 mm between the bump electrodes **70** on the semiconductor device **80** of this embodiment. Accordingly, the fusion or melting of the adjacent bumps can be reduced significantly which otherwise may occur during the formation of the bump electrodes. In addition, the semiconductor device according to the present invention can be mounted on, for example, a circuit board with a higher yield. Furthermore, the present process provides easier standardization of the semiconductor devices. This process also provides a higher reliability of the joint between the bump electrodes and the nickel or gold plating.

As mentioned above, according to the present invention, it is possible to mass-produce semiconductor devices without making a large investment for manufacturing facilities because the present process is in-line with a well-known chip manufacturing process. The semiconductor device obtained according to the present invention has a superior thermal stress resistance and good joints between the adjacent layers. This improves the moisture resistance of the semiconductor device.

While the present invention has thus been described in conjunction with a specific embodiment thereof, it is understood that the present invention is not limited to the illustrated embodiment. Instead, any changes, modifications, and variations may be made by those skilled in the art without departing from the scope and spirit of the appended claims. For example, gold may be used for the bumps rather than the solder. In such a case, the nickel plating and the gold plating can be eliminated.

What is claimed is:

1. A semiconductor wafer, including:

a plurality of the sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center.

2. A semiconductor wafer, including:

a plurality of chip sections defined thereon by scribe lines, each chip section having:

bump electrodes formed simultaneously thereon;

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center.

3. A semiconductor wafer including:

a plurality of chip sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum layer, wherein said plating contacts one of said bump electrodes and said aluminum layer contacts one of said chip electrodes.

4. A semiconductor wafer including:

a plurality of chip sections defined thereon by scribe lines, each chip section having:

bump electrodes formed simultaneously thereon;

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum, wherein said plating contacts said bump electrode and said aluminum layer contacts said chip electrode.

5. A semiconductor wafer as in claim 3, wherein said plating comprises one of nickel and copper.

6. A semiconductor wafer as in claim 3, wherein said aluminum layer has a thickness of no greater than 1 micrometer.

7. A semiconductor wafer as in claim 3, wherein said plating has a thickness of at least 5 micrometers.

8. A semiconductor wafer as in claim 3, further comprising a gold layer between said bump electrode and said plating.

9. A semiconductor wafer as in claim 1, wherein each of said chip sections has a center and a periphery and said interconnection layers extend from said periphery toward said center.

10. A semiconductor wafer as in claim 4, wherein said plating comprises one of nickel and copper.

11. A semiconductor wafer as in claim 4, wherein said aluminum layer has a thickness of no greater than 1 micrometer.

12. A semiconductor wafer as in claim 4, wherein said plating has a thickness of at least 5 micrometers.

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